On Automatic Fault Isolation Using DFT Methodology for Active Analog Filters

F.Novak, A.Biasizzo
Institute Jožef Stefan
Jamova 39, 61111 Ljubljana
Slovenia

M.Santo-Zarnik
Iskra HIPOT
68310 Šentjernej
Slovenia

I.Mozetič
Austrian Research Institute for AI
Schottengasse 3, A-1010 Vienna
Austria

Abstract

DFT methodology for active analog filters based on analog scan structures has been proposed by Soma. We describe an extension of the methodology to automatic fault isolation by means of model-based diagnosis performed by the AI tool CLP($\Re$). *The implemented diagnostic algorithm uses results of measurements of magnitude and phase characteristics for a given frequency in the normal mode and in the test modes. The diagnosis is performed incrementally, in each step reducing the set of potential candidates for the detected fault. Presented case study illustrates the approach.*

1 Introduction

In recent years, Artificial Intelligence (AI) systems for fault diagnosis are gaining considerable interest in practice. Employed methods are a subclass of SAT techniques and can be further divided into shallow and deep reasoning approaches. The deep or model-based reasoning approach uses behavioral circuit models in fault diagnosis. Promising results of this approach have been reported recently [2, 3].

In the paper we present an implementation and extension of the DFT methodology for active analog filters as proposed by Soma [4]. We use an AI tool CLP($\Re$) for modeling of analog filters, and model-based reasoning techniques combined with DFT for automatic fault isolation.

CLP($\Re$) is an instance of the Constraint Logic Programming (CLP) scheme [1]. In CLP is the unification mechanism, as used in Prolog, replaced by a more general operation — constraint satisfaction over specific domains. CLP($\Re$), for example, extends Prolog with interpreted arithmetic functions and a solver for systems of linear equations and inequalities over the domain of $\Re$eals. CLP($\Re$) is well suited to model real-valued system parameters with tolerances and feedback loops which in general cannot be resolved by local constraint propagation methods.

2 Diagnostic procedure

The main point of the referred DFT methodology is to introduce MOS switches to the filter circuit in order to increase its controllability and observability. The modified filter circuit can be tested in its normal mode of operation, in the all-test mode (with switches set to disconnect capacitors from the circuit), and in individual stage test modes.

The same modes of operation are used in the model-based diagnosis performed by CLP($\Re$). Hereby, the first task is to compose the model of the circuit and to confirm its correctness by satisfactory simulation results for the fault-free circuit operation in the normal mode. The modeling of analog circuits in CLP($\Re$) and its use for soft faults isolation is described in [3].

For given fault situation, measurements of gain and phase at selected test frequencies are performed on the experimental filter circuit. The results are compared to the simulated fault-free circuit output under the same input stimuli. If a fault is detected, a list of suspected faulty circuit components is given to CLP($\Re$) which computes the (deviating) values of the suspected components that might have caused the measured faulty circuit output. The values are computed for the normal mode, all-test mode, and each individual stage test mode, respectively. The mean value $\bar{x}$ and coefficients of variation V (i.e., $s/\bar{x}$) are computed for each suspected component in each operation mode, and for the composite case.

The next step is to reduce the list of suspected components. Components with computed negative values,

or with positive values exceeding possible practical range, or with large value of V are ruled out. Analysis of the all-test mode is performed in order to find out if the faulty component is resistance or capacitor. In the remaining list, the components with minimum value of V are declared as potentially faulty.

3 Experimental results

The low pass biquad filter, shown in Figure 1, has been implemented for experimental purposes in thick film hybrid technology. LS404C operational amplifiers and HEF4066B MOS switches were employed. HP4192 LF Impedance Analyzer was used for measuring gain and phase values in the range of 5Hz - 10kHz. CLP($\Re$) simulations were performed on SUN SPARCstation IPC. Obtained simulated values were close to the measured within less than 5%.

Detailed description of the CLP($\Re$) model of the filter together with the measurement and simulation results and computed diagnoses for different fault situations can be found in [5].

Let us briefly describe the case where $C_1 = 1$ nF is assumed instead of correct 100 nF. The Table presents the computed values of the suspected faulty components together with the corresponding coefficients of variation for the given operation modes.

Inspection of V in the normal mode immediately points to C_1 as being faulty because it has minimum V and its value differs by an order of magnitude from the other values. Nevertheless we proceed in order to illustrate the process of deriving the diagnosis as well as to confirm the initial result. R_4 can be ruled out due to the large value of its V in the normal mode. Simulation results [5] of the fault-free circuit in the all-test mode are close to the measured values. The situation implicitely indicates that fault can be expected in C_1 or C_2 since the circuit operates correctly if the capacitors are inactive. In the first stage test mode, R_3 is eliminated due to its V. Second stage test mode conclusions resemble the all-test mode case. Finally, the composite value V of C_1 is by an order of magnitude less than the other values which confirms previously stated diagnosis. Notice also, that the computed value of C_1 sufficiently resembles the actual value of the simulated fault in the experimental circuit.

Acknowledgements

The first three authors are supported by the Slovenian Ministry of Research and Technology, the last author is supported by the Austrian Federal Ministry of Science and Research.

References

[1] J.Cohen: Constraint logic programming languages. *Comm. of the ACM 33 (7)*, pp. 52-68, 1990.

[2] A.McKeon, A.Wakeling: Model-based analogue circuit fault diagnosis, *Proc. TEST90*, pp. 1-14, 1990.

[3] I.Mozetič, *et al.*: Model-based analogue circuit diagnosis with CLP($\Re$). *Proc. 4th Intl. GI Congress*, pp. 343-353, Munich, Springer-Verlag, 1991.

[4] M.Soma: A design-for-test methodology for active analog filters, *Proc. ITC 1990*, pp. 183-192.

[5] M. Santo - Zarnik, *et al.*: "Model-based fault diagnosis of active analog filters" *Techn. Report No. 6654*, Institute Jožef Stefan, 1993.

Suspected component	normal mode		all-test mode		1st stage test		2nd stage test		Composite value [Ω,nF]	Composite V
	[Ω,nF]	V	[Ω,nF]	V	[Ω,nF]	V	[Ω,nF]	V		
R_1	1546	0.876	83435	0.002	1832	0.862	99083	0.003	46474	1.039
R_2	277	0.497	11985	0.002	313	0.483	10092	0.003	5667	1.021
R_3	5548	0.419	2323	0.011	1	1.388	10006	0.000	4470	0.920
R_4	2369	41.420	59352	0.002	1668	0.504	49970	0.000	28340	1.801
R_5	277	0.495	11985	0.002	313	0.483	10092	0.003	5667	1.021
R_6	21202	0.431	8343	0.002	16974	0.435	9908	0.003	14107	0.506
C_1	1.16	0.063	x	x	1.21	0.021	x	x	1.19	0.045
C_2	2.71	0.507	x	x	x	x	1.01	0.003	5.18	1.094